WHAT IS CLAIMED IS:

1. A multi-state memory comprising:

a plurality of multi-state memory cells, each for storing one of a plurality of N multi-states;

at least one plurality of M populations of tracking cells, wherein each of said populations is associated with one of said multi-states, and wherein M is less than N; and

a read circuit for reading said multi-state memory cells using read points for each of said plurality of multi-states based upon the threshold voltages associated with the programmed state of said populations of tracking cells.

2. The multi-state memory of claim 1, wherein said memory cells are organized into a plurality of sectors, wherein each of said sectors has an associated plurality of M populations of tracking cells and a corresponding set of read points.

3. The multi-state memory of claim 2 further comprising a plurality of cells storing error correction code associated with each of said sectors.

4. The multi-state memory of claim 2, further comprising:

a programming circuit for writing data values to said memory cells and for programming said tracking cells.

5. The multi-state memory of claim 4, wherein said programming circuit includes a verify circuit using a set of fixed reference values for program verify for writing data values to said memory cells and the same set of fixed reference values for program verify for programming said tracking cells.

6. The multi-state memory of claim 5, wherein a tracking cell which fails to be verified by the verify circuit when programming said tracking cells is removed from said populations of tracking cells.

7. The multi-state memory of claim 5, wherein said programming circuit writes said memory cells and programs said tracking cells within a sector concurrently.

8. The multi-state memory of claim 1, wherein said read circuit comprises:

tracking cell read circuitry for reading threshold voltages associated with the programmed state of said tracking cells;

a memory controller for establishing the read points for each of said plurality of multi-states based upon said threshold voltages read from said populations of tracking cells.

9. The multi-state memory of claim 8, wherein said memory controller further manages the multi-state memory and transfers data between the memory and a host system to which it is connected.

10. The multi-state memory of claim 8, wherein said memory controller forms part of the same integrated circuit as said memory cells and said populations of cells tracking cells.

11. The multi-state memory of claim 8, wherein said memory controller forms part of an integrated circuit separate from said memory cells and said populations of cells tracking cells.

12. The multi-state memory of claim 11, wherein said read circuit further comprises:

a fast look-up table for storing said the read points established by said memory controller, wherein the fast look-up table forms part of the same integrated circuit as said memory cells and said populations of cells tracking cells, and wherein the multi-state memory cells are read using the fast look-up table.

13. The multi-state memory of claim 1, wherein each of said populations of tracking cells comprises a plurality of tracking cells.

14. The multi-state memory of claim 13, wherein M is equal to two.

15. A multi-state memory comprising:

a plurality of multi-state memory cells, each for storing one of a plurality N of multi-states;

a plurality M of populations of tracking cells, wherein each of said populations is associated with one of said multi-states; and

a read circuit for reading said multi-state memory cells using read points for distinguishing between adjacent states of said plurality of multi-states based upon threshold voltages read from said populations of tracking cells, wherein at least one of said read points is based upon threshold voltages from a population of tracking cells not associated with the adjacent states between which said at least one read point distinguishes.

16. The multi-state memory of claim 15, wherein said memory cells are organized into a plurality of sectors, wherein each of said sectors has an associated plurality of M populations of tracking cells and a corresponding set of read points.

17. The multi-state memory of claim 16 further comprising a plurality of cells storing error correction code associated with each of said sectors.

18. The multi-state memory of claim 16, further comprising:

a programming circuit for writing data values to said memory cells and for programming said tracking cells.

19. The multi-state memory of claim 18, wherein said programming circuit includes a verify circuit using a set of fixed reference values for program verify for writing data values to said memory cells and the same set of fixed reference values for program verify for programming said tracking cells.

20. The multi-state memory of claim 19, wherein a tracking cell which fails to be verified by the verify circuit when programming said tracking cells is removed from said populations of tracking cells.

21. The multi-state memory of claim 19, wherein said programming circuit writes said memory cells and programs said tracking cells within a sector concurrently.

22. The multi-state memory of claim 15, wherein said read circuit comprises:

tracking cell read circuitry for reading threshold voltages associated with the programmed state of said tracking cells;

a memory controller for establishing said read points for each of said plurality of multi-states based upon said threshold voltages read from said populations of tracking cells.

23. The multi-state memory of claim 22, wherein said memory controller further manages the multi-state memory and transfers data between the memory and a host system to which it is connected.

24. The multi-state memory of claim 22, wherein said memory controller forms part of the same integrated circuit as said memory cells and said populations of cells tracking cells.

25. The multi-state memory of claim 22, wherein said memory controller forms part of an integrated circuit separate from said memory cells and said populations of cells tracking cells.

26. The multi-state memory of claim 25, wherein said read circuit further comprises:

a fast look-up table for storing said the read points established by said memory controller, wherein the fast look-up table forms part of the same integrated circuit as said memory cells and said populations of cells tracking cells, and wherein the multi-state memory cells are read using the fast look-up table.

27. The multi-state memory of claim 15, wherein each of said populations of tracking cells comprises a plurality of tracking cells.

28. The multi-state memory of claim 27, wherein M is equal to two.

29. A multi-state memory comprising:

a plurality of multi-state memory cells, each for storing one of a plurality N of multi-states;

a plurality M of tracking cell populations, wherein each of said populations is associated with one of said multi-states; and

a translation circuit for reading said multi-state memory cells using read points for each of said plurality of multi-states using the analog value of the programmed state of said tracking cell populations.

30. The multi-state memory of claim 29, wherein each of said plurality M of tracking cell populations is comprised of a plurality of tracking cells.

31. The multi-state memory of claim 30, wherein said memory cells are organized into a plurality of sectors, wherein each of said sectors has an associated plurality of M of tracking cell populations and a corresponding set of read points.

32. The multi-state memory of claim 31 further comprising a plurality of cells storing error correction code associated with each of said sectors.

33. The multi-state memory of claim 31, further comprising:

a programming circuit for writing data values to said memory cells and for programming said tracking cells.

34. The multi-state memory of claim 33, wherein said programming circuit includes a verify circuit using a set of fixed reference values for program verify for writing data values to said memory cells and the same set of fixed reference values for program verify for programming said tracking cells.

35. The multi-state memory of claim 34, wherein a tracking cell which fails to be verified by the verify circuit when programming said tracking cells is removed from said populations of tracking cells.

36. The multi-state memory of claim 34, wherein said programming circuit writes said memory cells and programs said tracking cells within a sector concurrently.

37. The multi-state memory of claim 30, wherein said translation circuit comprises:

a read point circuit for establishing at least (N-1) read points using an analog value from each of said M tracking cell populations; and

a read/verify circuit connected to receive said at least (N-1) read points and read said multi-state memory cells by comparing said read points to the threshold voltages of said multi-state memory cells.

38. The multi-state memory of claim 37, wherein said comparing is a binary search.

39. The multi-state memory of claim 37, further comprising:

a plurality M of averaging circuits, each connectable to the tracking cells of one of said plurality of tracking cell populations to form an average of the analog threshold values of the tracking cells of said one of said plurality of tracking cell populations and supply said analog value from each of said M tracking cell populations to said read point circuit.

40. The multi-state memory of claim 39, wherein M is equal to 2.

41. The multi-state memory of claim 39, wherein said average is an arithmetic mean.

42. The multi-state memory of claim 37, further comprising:

a programming circuit for writing data values to said memory cells and for programming said tracking cells; and

a reference value circuit connected to supply M voltage levels to said read point circuit, wherein said M voltage levels are independent of the threshold voltages of said tracking cells, and wherein said read point circuit is connected to supply program verify levels to said read /verify circuit for use in writing data values to said memory cells and for programming said tracking cells.

43. The multi-state memory of claim 38, wherein program verify levels include a marginning level.

44. The multi-state memory of claim 29, further comprising:

a rotation circuit for altering the multi-state with which each of said populations is associated.

45. A non-volatile memory comprising:

a plurality of memory cells, each for storing one of N states;

a plurality of tracking cells, wherein each of said tracking cells is associated with one of said N states;

a read circuit for reading said memory cells using read points for each of said N states based upon the threshold voltages associated with the programmed state of said tracking cells; and

programming circuitry for programming said memory cells and said tracking cells, wherein at least one of said tracking cells is programmed by a different algorithm than a memory cell programmed to the associated one of said N states.

46. The non-volatile memory of claim 45, wherein said at least of said tracking cells is programmed by using pulses of a shorter duration than are used for a memory cell programmed to the associated one of said N states.

47. The non-volatile memory of claim 45, wherein said at least of said tracking cells is programmed by using a control gate voltage have a lower magnitude than is used for a memory cell programmed to the associated one of said N states.

48. The non-volatile memory of claim 45, wherein said at least of said tracking cells is programmed by using a drain voltage have a lower magnitude than is used for a memory cell programmed to the associated one of said N states.

49. The non-volatile memory of claim 45, wherein said tracking cells are programmed concurrently with said memory cells.

50. The non-volatile memory of claim 45, wherein said memory cells are multi-state memory cells, N being greater than two.

51. The non-volatile memory of claim 50, wherein said tracking cells form a plurality M of tracking cell populations, each comprised of a plurality of tracking cells, wherein each of said populations is associated with one of said multi-states.

52. The non-volatile memory of claim 51, wherein M is less than N.

53. The non-volatile memory of claim 52, wherein M is two.

54. The non-volatile memory of claim 45, wherein said programming circuit includes a verify circuit using a set of fixed reference values for program verify for programming said memory cells and the same set of fixed reference values for program verify for programming said tracking cells.

55. The multi-state memory of claim 54, wherein a tracking cell which fails to be verified by the verify circuit when programming said tracking cells is removed from said plurality of tracking cells.

56. A method of operating a multi-state memory comprising:

reading the threshold voltages of one or more multi-state memory cells, each for storing one of a plurality N of multi-states;

reading the threshold voltages of a plurality M of populations of tracking cells, wherein each of said populations is associated with one of said multi-states, and wherein M is less than N; and

converting the threshold voltages of said memory cells to logical values of said plurality of multi-states using the threshold voltages of said tracking cells.

57. The method of claim 56, wherein said converting comprises:

determining from the threshold voltages of said tracking cells a relation between the threshold voltages of said memory cells and the logical value of said plurality of multi-states; and

translating the threshold voltages of said memory cells to logical values of said plurality of multi-states using said relation.

58. The method of claim 57, wherein said converting further comprises:

storing said relation in a fast look-up table for use in said translating, wherein said fast look-up table comprises part a single integrated circuit with said memory cells.

59. The method of claim 58, further comprising:

shifting said logical values from said integrated circuit, wherein said translating is performed concurrently with the shifting.

60. The method of claim 57, wherein said relation is a curve of degree (M−1).

61. The method of claim 57, wherein said relation is piece-wise linear.

62. The method of claim 57, wherein each of said plurality of populations contains a plurality of tracking cells.

63. The method of claim 62, wherein said determining a relation comprises:

establishing an average threshold value associated with each of said populations of tracking cells; and

determining said relation from said average threshold values.

64. The method of claim 63, wherein each of the average threshold values are established only form those tracking cells in the associated population whose threshold values differ from the average threshold value by less than a specified bound.

65. The method of claim 63, wherein said relation is linear.

66. The method of claim 65, wherein M is equal to two.

67. The method of claim 57, wherein said determining includes establishing a correspondence to determine for each of said populations of tracking cells the multi-state with which it is associated.

68. The method of claim 67, wherein said translating includes establishing the rotation of said logical value between the threshold voltages of said memory cells based upon said correspondence.

69. The method of claim 56, further comprising:

programming said memory cells prior to said reading the threshold voltages of one or more multi-state memory cells; and

programming said tracking cells prior to said reading the threshold voltages of said tracking cells, wherein each of said populations of tracking cells is programmed using the same program verify level as a memory cell programmed to the multi-state with which it is associated.

70. The method of claim 69, further comprising:

removing from said populations of tracking cells a tracking cell which fails to be verified when programming said tracking cells.

71. The method of claim 69, wherein the multi-state with which each of said populations of tracking cells is associated is predetermined.

72. The method of claim 56, further comprising:

reading the threshold voltages of one or more cells storing error correction code;

converting the threshold voltages of said one or more cells storing error correction code to a correction code using the threshold voltages of said tracking cells; and

operating on the logical values of said plurality of multi-states using the correction code to obtain corrected values of said logical values.

73. A method of operating a multi-state memory comprising:

reading the threshold voltages of one or more multi-state memory cells, each for storing one of a plurality N of multi-states;

reading the threshold voltages of a plurality M of populations of tracking cells, wherein each of said populations is associated with one of said multi-states;

establishing read points for distinguishing between adjacent states of said plurality of multi-states based upon the threshold voltages of said populations of tracking cells, wherein at least one of said read points is based upon the threshold voltages from a population of tracking cells not associated with the adjacent states between which said at least one read point distinguishes; and

converting the threshold voltages of said memory cells to logical values of said plurality of multi-states using said read points.

74. The method of claim 73, wherein said establishing read points comprises:

determining from the threshold voltages of said tracking cells a relation between the threshold voltages of said memory cells and the logical value of said plurality of multi-states; and

translating said relation into said read points.

75. The method of claim 74, wherein said converting further comprises:

storing said relation in a fast look-up table for use in said translating, wherein said fast look-up table comprises part a single integrated circuit with said memory cells.

76. The method of claim 75, further comprising:

shifting said logical values from said integrated circuit, wherein said translating is performed concurrently with the shifting.

77. The method of claim 74, wherein said relation is a curve of degree (M-1).

78. The method of claim 74, wherein said relation is piece-wise linear.

79. The method of claim 74, wherein each of said plurality of populations contains a plurality of tracking cells.

80. The method of claim 79, wherein said determining a relation comprises:

establishing an average threshold value associated with each of said populations of tracking cells; and

determining said relation from said average threshold values.

81. The method of claim 80, wherein each of the average threshold values are established only form those tracking cells in the associated population whose threshold values differ from the average threshold value by less than a specified bound.

82. The method of claim 80, wherein said relation is linear.

83. The method of claim 82, wherein M is equal to two.

84. The method of claim 74, wherein said determining includes establishing a correspondence to determine for each of said populations of tracking cells the multi-state with which it is associated.

85. The method of claim 84, wherein said translating includes establishing the rotation of said logical value between the threshold voltages of said memory cells based upon said correspondence.

86. The method of claim 73, further comprising:

programming said memory cells prior to said reading the threshold voltages of one or more multi-state memory cells; and

programming said tracking cells prior to said reading the threshold voltages of said tracking cells, wherein each of said populations of tracking cells is programmed using the same program verify level as a memory cell programmed to the multi-state with which it is associated.

87. The method of claim 86, further comprising:

removing from said populations of tracking cells a tracking cell which fails to be verified when programming said tracking cells.

88. The method of claim 86, wherein the multi-state with which each of said populations of tracking cells is associated is predetermined.

89. The method of claim 73, further comprising:

reading the threshold voltages of one or more cells storing error correction code;

converting the threshold voltages of said one or more cells storing error correction code to a correction code using the threshold voltages of said tracking cells; and

operating on the logical values of said plurality of multi-states using the correction code to obtain corrected values of said logical values.

90. A method of operating a multi-state memory comprising:

providing one or more multi-state memory cells, each for storing one of a plurality N of multi-states;

providing a plurality M of tracking cell populations, wherein each of said populations is associated with one of said multi-states; and

establishing (N-1) read points using the analog value of the programmed state of said tracking cell populations; and

converting the threshold voltages of said memory cells to logical values of said plurality of multi-states using said read points.

91. The method of claim 90, wherein each of the tracking cell populations is comprised of a plurality of tracking cells,.

92. The method of claim 91, wherein said establishing read points comprises:

determining from the threshold voltages of said tracking cells a relation between the threshold voltages of said memory cells and the logical value of said plurality of multi-states; and

translating said relation into said read points.

93. The method of claim 92, wherein said relation is a curve of degree (M-1).

94. The method of claim 92, wherein said relation is piece-wise linear.

95. The method of claim 91, wherein said determining a relation comprises:

establishing an average threshold value associated with each of said populations of tracking cells; and

determining said relation from said average threshold values.

96. The method of claim 95, wherein said relation is linear.

97. The method of claim 96, wherein M is equal to two.

98. The method of claim 91, further comprising:

programming said memory cells prior to said reading the threshold voltages of one or more multi-state memory cells; and

programming said tracking cells prior to said reading the threshold voltages of said tracking cells, wherein each of said populations of tracking cells is programmed using the same program verify level as a memory cell programmed to the multi-state with which it is associated.

99. The method of claim 98, further comprising:

removing from said populations of tracking cells a tracking cell which fails to be verified when programming said tracking cells.

100. The method of claim 98, wherein the multi-state with which each of said populations of tracking cells is associated is predetermined.

101. The method of claim 90, further comprising:

plurality of cells storing error correction code;

converting the threshold voltages of said one or more cells storing error correction code to a correction code using said read points; and

operating on the logical values of said plurality of multi-states using the correction code to obtain corrected values of said logical values.

102. The method of claim 90, wherein said establishing (N-1) read points includes determining a correspondence to determine for each of said populations of tracking cells the multi-state with which it is associated.

103. The method of claim 102, wherein said converting includes establishing the rotation of said logical value between the threshold voltages of said memory cells based upon said correspondence.

104. A method of operating a non-volatile memory comprising:

programming one or more memory cells, each for storing one of N states;

programming a plurality of tracking cells, wherein each of said tracking cells is associated with one of said N states, wherein at least one of said tracking cells is programmed by a different algorithm than a memory cell programmed to the associated one of said N states; and

converting the threshold voltages of said memory cells to logical values of said N states using the threshold voltages of said tracking cells.

105. The method of claim 104, wherein each of said plurality of tracking cells is programmed using the same program verify level as a memory cell programmed to the state with which it is associated.

106. The method of claim 105, further comprising:

removing from said populations of tracking cells a tracking cell which fails to be verified when programming said tracking cells.

107. The method of claim 104, wherein said programming a plurality of tracking cells uses pulses of a shorter duration than are used for said programming one or more memory cells.

108. The method of claim 104, wherein said programming a plurality of tracking cells uses a control gate voltage having a lower magnitude than is used for said programming one or more memory cells.

109. The method of claim 104, wherein said programming a plurality of tracking cells uses a drain voltage having a lower magnitude than is used for said programming one or more memory cells.

110. The method of claim 104, wherein said programming a plurality of tracking cells and said programming one or more memory cells are performed concurrently.

111. The method of claim 104, wherein said converting comprises:

determining from the threshold voltages of said tracking cells a relation between the threshold voltages of said memory cells and the logical value of said N states; and

translating the threshold voltages of said memory cells to logical values of said N states using said relation.

112. The method of claim 111, wherein said memory cells are multi-state memory cells, N being greater than two.

113. The method of claim 112, wherein said tracking cells form a plurality M of tracking cell populations, each comprised of a plurality of tracking cells, wherein each of said populations is associated with one of said multi-states.

114. The method of claim 113, wherein M is less than N.

115. The method of claim 114, wherein M is two.

116. An integrated circuit comprising:

a plurality of multi-state memory cells, each for storing one of a plurality N of data states;

a plurality of M reference voltage circuits, wherein each reference voltage circuit is associated with one of said N data states, and each comprising:

a population of tracking cells; and

a dedicated sense amp for each of said tracking cells connected to provide an analog voltage associated with the programmed state of the tracking to which it is connected;

a read point circuit connected to said reference voltage circuits to receive said analog values and providing at least (N-1) voltage levels derived from said average values; and

reading circuitry connected to receive said at least (N-1) voltage levels and connectable to said memory cells and providing the data state of a memory cell to which it is connected based on said at least (N-1) voltage levels.

117. The integrated circuit of claim 116, wherein each of said populations comprise a plurality of tracking cells, and wherein each of the plurality of M reference voltage circuits further comprises:

an averaging circuit connectable to each of said sense amps to receive the corresponding analog voltages and providing an averaged value of said analog voltages, and wherein the analog values received by the read point circuit are said averaged values.

118. The integrated circuit of claim 117, wherein each of said sense amps comprise:

a first transistor connected between a voltage source and a first node and having a control gate connected to a reference voltage;

a second transistor connected between said voltage source and a second node and having a control gate connected to said first node;

a third transistor connected between said second node and ground; and

an output for providing said analog voltage connected to said second node, wherein the tracking cell connected to the sense amp is connected between said first node and ground and has a control gate connected to said second node.

119. The integrated circuit of claim 118, the sense amp further comprising:

at least one cascode device connected between said first transistor and said first node; and

at least one cascode device connected between said first node and said tracking cell connected to the sense amp.

120. The integrated circuit of claim 117, wherein each reference voltage circuit further comprises:

a plurality of switches, one for each of said plurality of tracking cells, each connected between the corresponding one of said dedicated sense amps and said averaging circuit to disconnect said corresponding sense amp form said averaging circuit.

121. The integrated circuit of claim 117, wherein read point circuit comprises:

a chain of resistive elements connected between a first and second voltage level, having at least (N-1) nodes between said resistive elements corresponding to said at least (N-1) voltage levels and M nodes to which said averaged values are connectable.

122. The integrated circuit of claim 121, wherein each of said averaged values are connectable to said chain of resistive elements through a buffering element.

123. The integrated circuit of claim 121, further comprising:

a rotation circuit for permuting which of said M nodes is connected to which of said averaged values.

124. The integrated circuit of claim 121, wherein M is equal to two.

125. The integrated circuit of claim 124, further comprising:

programming circuitry connected to said memory cells and said tracking cells;

a verify reference voltage generating circuit connected to provide a pair of verify voltages connectable to said pair of nodes to which said averaged values are connectable, wherein in response to control signal during a programming process said averaged values are disconnected from said pair of nodes and said verify voltages are connected, thereby providing at least (N-1) program verify voltages to said reading circuitry.

126. The integrated circuit of claim 125, wherein said programming circuitry programs said memory cells concurrently with said tracking cells using said at least (N-1) program verify voltages.

127. The multi-state memory of claim 126, wherein a tracking cell which fails to be verified when programming said tracking cells is removed from said populations of tracking cells.

128. A said sense amp for providing the analog voltage level of a non-volatile memory cell connected between said sense amp and ground, comprising:

a first transistor connected between a voltage source and a first node and having a control gate connected to a reference voltage;

a second transistor connected between said voltage source and a second node and having a control gate connected to said first node;

a third transistor connected between said second node and ground; and

an output for providing said analog voltage connected to said second node, wherein said memory cell is connected between said first node and ground and has a control gate connected to said second node.

129. The sense amp of claim 128, further comprising:

at least one cascode device connected between said first transistor and said first node; and

at least one cascode device connected between said first node and said tracking cell connected to the sense amp.